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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,470	09/08/2003	Naoto Hirota	KANEKO.008AUS	9817
7590	10/04/2010		EXAMINER	
MURAMATSU & ASSOCIATES 114 PACIFICA SUITE 310 Irvine, CA 92618				CALEY, MICHAEL H
ART UNIT		PAPER NUMBER		
2871				
MAIL DATE		DELIVERY MODE		
10/04/2010		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/657,470	HIROTA, NAOTO	
	<b>Examiner</b>	<b>Art Unit</b>	
	MICHAEL H. CALEY	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 19 October 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1,3,4,6,7,9,10,12,13,15,16 and 18-54 is/are pending in the application.  
 4a) Of the above claim(s) 9,10,12,13,15,16 and 18-52 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,3,4,6,7,53 and 54 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 08 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/09 has been entered.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S.**

**Patent Application Publication No. 2003/0112397).**

Regarding claim 1, Suzuki discloses a color active matrix type vertically aligned mode liquid crystal display comprising on a substrate:

- a scan signal wiring (Figure 3 element 14);
- a video signal wiring (Figure 3 element 17);

a thin film transistor (TFT) which is formed at an intersection of the scan signal wiring and the video signal wiring;

a transparent pixel electrode (13; Paragraph [0049]) connected to the thin film transistor (Figure 3) element in which two or more long and slender slits are formed (16', 16);

an active matrix substrate (Figures 1, 2, element 11) having a liquid crystal alignment direction control electrode (18) in a lower layer of the slits of the transparent pixel electrode currently formed via an insulator film (15);

a substrate (10) facing the active matrix substrate; and

an anisotropic liquid crystal layer (100) having a negative dielectric constant (Paragraph [0049]);

wherein in order to impress a voltage to liquid crystal molecules vertically aligned (Paragraph [0051]) between the active matrix substrate and the other substrate, and to make the liquid crystal molecules tilt in different two directions (Figures 1 and 2), two kinds of following electrode structures are formed in one pixel of the active matrix substrate:

(i) an electrode structure in which a transparent flat common electrode (12) is used on the other substrate side, and for the transparent pixel electrodes facing the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed (16') in such a way that the transparent pixel electrode is removed at a part of the slit, where the liquid crystal alignment direction control electrode is excluded in a lower layer of the slit (Figures 3 and 4 element 16');

(ii) an electrode structure in which a transparent flat common electrode is used in the other substrate side, and for the transparent pixel electrode facing the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slits and a larger dimension than a dimension of the slits is formed in a lower layer of the slits (Figures 1-4 elements 16 and 18) via the insulator film (15) where the transparent pixel electrode and the liquid crystal alignment direction control electrode in each pixel of the active matrix substrate are driven separately from one another (Paragraph [0057]).

Regarding claim 7, Lee discloses adjacent transparent pixel electrodes in a direction of the scan signal wiring are connected to a thin film transistor component controlled by mutually different scan signal wirings (Paragraph [0050]).

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 4, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Watanabe.**

Lee fails to disclose the polarities of the potential of the transparent pixel electrode, and the potential of the liquid crystal alignment control electrode as reversed to a polarity of the potential of the flat common electrode in the color filter substrate side every vertical scanning period. Watanabe, however, teaches such a reversal of polarity for every vertical scanning period as a means of reducing flicker (Column 3 lines 39-42, Column 4 lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to drive the display disclosed by Lee by reversing the polarity in every vertical scanning period. One would have been motivated to drive the display as proposed to reduce display flicker (Watanabe Column 3 lines 39-42, Column 4 lines 45-62).

Lee as modified by Watanabe further discloses two rows of liquid crystal alignment direction control electrodes that are mutually separated and set at potentials different from each other and as mutually exchanged in every fixed pixel cycle, due to polarity inversion between pixels.

**Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable Lee in view of Suzuki et al. (U.S. Patent No. 6,407,791 “Suzuki”) and Watanabe (U.S. Patent No. 6,665,023).**

Regarding claim 3, Lee fails to disclose the driving characteristics as proposed.

Suzuki discloses the display such that:

when a potential of the transparent pixel electrode separated for every pixel of the active matrix substrate side is lower than a potential of the facing flat common electrode

on the color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode (Column 11 lines 1-8, Column 11 lines 24-31); and

when a potential of the transparent pixel electrode separated for every pixel of the active matrix substrate side is higher than a potential of the facing flat common electrode on the color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode (Column 11 lines 1-8, Column 11 lines 24-31).

Further, Watanabe, however, teaches such a reversal of polarity for every vertical scanning period as a means of reducing flicker (Column 3 lines 39-42, Column 4 lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to drive the display disclosed by Lee by setting the potential of the transparent pixel electrode and the liquid crystal alignment electrode relative to one another as proposed and reversing the polarity in every vertical scanning period. One would have been motivated to set the liquid crystal alignment direction control electrode as proposed to cause the liquid crystal to be aligned for a symmetric viewing angle characteristic (Column 11 lines 45-49). One would have been motivated to drive the display with the proposed reversal of polarity to reduce display flicker (Watanabe: Column 3 lines 39-42, Column 4 lines 45-62).

***Response to Arguments***

Applicant's arguments with respect to claims 1, 3, 4, 6, 7, 53, and 54 have been considered but are moot in view of the new ground(s) of rejection.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 6:00 a.m - 2:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871